IN THE CLAIMS

Claims 1-18 Cancelled.

19. (Currently Amended) A method of automatically generating a test environment for an ATE, designed to test a single integrated circuit, the method comprising the steps of:

mapping the pins of the ATE to a plurality of integrated circuits to create pin data;

automatically generating, with a test program generator, a test program and testpattern data for the integrated circuits from pattern data, generic test program rules, and the pin data; and

executing the test program to control the ATE, the test program appearing to the ATE as a test for a single integrated circuit.

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20. (Original) The method of claim 19 further comprising the step of:

generating functional fail data for each of the integrated circuits.

21. (Currently Amended) The method of claim ~~1~~ 19 wherein the test program includes test vectors and pin assignments for testing the integrated circuits in parallel.

22. (Original) An automated test system comprising:

an integrated circuit tester designed to test a single integrated circuit;

a pin data storage area capable of containing pin data for mapping a plurality of integrated circuits to the pins of the integrated circuit tester;

a generic program rules storage area; and

a test program generator capable of generating a test program from the pin data, test pattern data and generic program rules, the test program capable of controlling the integrated circuit tester for testing the integrated circuits in parallel.

23. (Original) The automated test system of claim 22 further comprising:

a storage area capable of storing fail data generated during testing for each one of the integrated circuits.

24. (Original) The automated test system of claim 22 wherein the test program includes test vectors and pin

assignments for testing the integrated circuits in parallel.

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25. (Currently Amended) A computer progam product comprising:

a computer usable medium having computer readable program code embodied in the medium for automatically generating a test environment for an integrated circuit tester when executed, the computer readable program code including:

computer readable program code that is capable of mapping the pins of the integrated circuit tester to a plurality of integrated circuits to create pin data; and

computer readable program code that is capable of automatically generating, with a test program generator, a test program and test pattern data ~~fro~~ for the integrated circuits from pattern data, generic test program rules, and the pin data, the test program appearing to the integrated circuit tester as a test for a single integrated circuit.

26. (Original) The computer program product of claim 25 wherein the computer readable program code further includes:

computer readable program code capable of generating functional fail data for each of the integrated circuits.

27. (Original) The computer program product of claim 25 wherein the test program includes test vectors and pin assignments for testing the integrated circuits in parallel.

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28. (New) A method of automatically generating a test environment for an ATE, the method comprising the steps of:

mapping the pins of the ATE to a plurality of integrated circuits to create pin data;

automatically generating, with a test program generator, a test program and testpattern data for each one of the integrated circuits from pattern data, generic test program rules, and the pin data, the test program appearing to the ATE as a test program for a single integrated circuit; and

executing the test program to control the ATE.

CLAIM OBJECTIONS

The Examiner objected to claim 21 as depending from cancelled claim 1. Claim 21 has been amended to properly depend from independent claim 19.

REJECTION OF CLAIMS 19-27 UNDER 35 U.S.C. SECTION 102(e)

In the current Office Action, the Examiner rejected claims 19-27 under 35 U.S.C. Section 102(e) as being anticipated by U.S. Patent No. 6557128 B1 to Turnquist ("Turnquist").

Turnquist discloses a ATE that is modified using specialized hardware (pin-unit/system controller interface 32) to allow simultaneous testing of multiple integrated circuits (DUTs) (see Col. 4 lines 23-30 and corresponding Figure 3, Col. 4 lines 44-49). The specialized hardware allows Turnquist to group pins together for virtual testers. Turnquist, however, fails to disclose, teach or suggest the use of an ATE designed to test a single integrated circuit.

Applicant's present invention, as now defined by the pending claims, is a method of converting an ATE that is designed to test a single integrated circuit at a time, to an ATE that is capable of testing a plurality of integrated circuits in parallel. Specifically, Applicant's present invention automatically creates a test program that runs on the ATE such that the program appears to the ATE as if it were written to test a single integrated circuit. The test program, however, has code that allows it to assign the pins of the ATE to specific tasks associated with one of the integrated circuits.

In contrast, Turnquist modifies/converts an ATE to use specialized hardware to make the ATE capable of testing multiple integrated circuits in parallel. As such, Turnquist fails to teach or suggest the creation of a test program that appears to the ATE as if it were written to test a single integrated circuit.

SUMMARY AND CONCLUSION